IN THE DRAWINGS

Please amend the drawings as follows:

In FIG. 6C, please change reference number "528" to reference numeral --528/234--; please change reference number "540" to reference numeral --540/236--; and please identify the data bus with reference numeral --510--.

In FIG. 8C, please change reference number "830" to reference numeral --850--.

In FIG. 9, please identify the accumulator with reference numeral --526--.

REMARKS

Claims 1-39, 43, 44, 47-54 and 57-59 were pending in the present application. Claims 1, 2, 4-9, 15, 16, 22, 26, 27, 29, 32-39, 43, 48, 49, 53, 54 and 57 have been amended. Claims 3, 47 and 59 have been canceled without prejudice. Claims 40-42, 45, 46 and 55-56 were previously canceled without prejudice. New Claims 60 and 61 have been added.

Applicants thank the Examiner for allowing Claims 15 and 35. Claims 4-14, 16-32, 34 and 36-39 have been amended to depend directly or indirectly from allowed Claim 35. New Claim 60 also depends from allowed Claim 35. Also, independent method Claim 48 has been amended to include limitations from allowed Claim 35. Method Claims 49-54 depend directly or indirectly from Claim 48. Applicants respectfully request allowance of these Claims 4-32, 34-39, 48-54 and 60.

The remarks below relate to the remaining claims, which are amended Claim 1, 2, 33, 43, 44, 57, 58 and 61.

Claim 1 has been amended to clarify one embodiment. Amended Claim 1 is fully supported by the specification. The "first buffer" and its limitations in Claim 1 are supported by at least Fig. 6A, original Claim 1, original Claim 40 and the specification.

The "data processor" and its limitations in Claim 1 are supported by at least Figs. 5-11B; p. 3, lines 7-30; p. 11, lines 1-3, 14-15, 29-36; p. 18, lines 22-27; p. 21, lines 1-11; and original Claims 2-54.

The "controller" and the "address generator" and their limitations in Claim 1 are supported by at least Figs. 5, 6C, and 10; p. 5, lines 12-14; p. 10, lines 2-12; p. 18, lines 19-27; p. 20, lines 18 to p. 21, line 13; p. 35, lines 15-27; and original claims 2-6, 35.

The "microcontroller" and its limitations in Claim 1 are supported by at least Figs. 5 and 10; p. 34, line 12 to p. 36, line 3; and original claims 33-35.

The Sept. 7, 2004 Office Action rejected Claims 1-14, 16-34, 36-39, 43, 44, 47-54, 57 and 58 under 35 U.S.C. § 112, first paragraph, for failing to comply with the enablement requirement. The Office Action asserted that the specification does not describe a data processor processing "two or more" retrieved segments "at different times with the same corresponding despreading sequence."

Applicants respectfully traverse this rejection. The "data processor coupled to the first buffer and operative to (a) retrieve different segments of the digitized samples one segment at a time from the first buffer, each of the retrieved segments comprising one of the multiple signal instances, (b) process two or more of the retrieved segments one segment at a time with one programmed despreading sequence" in amended Claim 1 is supported by the specification, p. 12, line 38 to p. 13, line 6; p. 20, line 37 to p. 21, line 7; p. 36, lines 4-26 and Fig. 11A.

The Office Action rejected Claims 1-14, 16-34, 36-39, 43, 44, 47-54, 57 and 58 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Claim 1 has been amended to remove "the same corresponding segment."

The Office Action rejected Claims 1-3, 7-10, 12, 13, 25, 38, 47-49 and 58 under 35 U.S.C. § 102(a) as being anticipated by Lee (EP 1017183A2).

Lee does not disclose or teach "a data processor ... operative to (a) retrieve different segments of the digitized samples one segment at a time from the first buffer, each of the retrieved segments comprising one of the multiple signal instances," as recited in Claim 1. Lee also does not disclose a "data processor ... operative to ... decover the despread samples with a channelization code of programmable length to provide decovered symbols," as recited in Claim 1.

Lee also does not disclose:

"a controller being operative to direct the data processor;

a microcontroller coupled to the data processor and the controller, the microcontroller being operative to receive tasks from the controller, instantiate a state machine for each task, and direct the data processor to process the retrieved multiple segments; and

an address generator coupled to the first buffer and the controller, the address generator being operative to implement a counter to control a write address for writing digitized samples to the first buffer, the counter being operative to send a signal to the controller to initiate processing of the stored samples by the data processor,"

as recited in Claim 1. Claims 2, 33, 43, 44, 57, 58 depend from Claim 1. Claim 61 recites limitations similar to Claim 1. Thus, Claims 1, 2, 33, 43, 44, 57, 58 and 61 should be allowable over Lee.

The Office Action rejected Claims 1-3, 7-13, 23-26, 32, 36-38, 43, 44, 47-49, 54, and 58 under 35 U.S.C. § 102(a) as being anticipated by Kawabe et al. (EP 0998052A2).

Kawabe discloses multiple "despreading" blocks or "correlators" 208-1 through 208-n and multiple "detection" blocks 211-1 through 211-n in Fig. 1 and col. 6, paragraph 0033. The Background and the Summary of the present application explains that multiple, dedicated processing elements, such as 208-1 through 208-n and 211-1 through 211-n in Kawabe, assigned to process specific signal instances is inefficient, non-programmable, not scalable to handle more signal instances, and increases complexity and costs. See e.g., Background p. 1, line 32 to p. 2, line 16.

Kawabe does not disclose or teach a single "data processor coupled to the first buffer and operative to (a) retrieve different segments of the digitized samples one segment at a time from the first buffer, each of the retrieved segments comprising one of the multiple signal instances, (b) process two or more of the retrieved segments one segment at a time with one programmed despreading sequence to provide despread samples, (c) decover the despread samples with a channelization code of programmable length to provide decovered symbols, (d) demodulate the decovered symbols to provide demodulated symbols, and (e) combine the demodulated symbols from multiple signal instances to provide processed symbols.

Kawabe also does not disclose or teach:

"a controller being operative to direct the data processor;

a microcontroller coupled to the data processor and the controller, the microcontroller being operative to receive tasks from the controller, instantiate a state machine for each task, and direct the data processor to process the retrieved multiple segments; and

an address generator coupled to the first buffer and the controller, the address generator being operative to implement a counter to control a write address for writing digitized samples to the first buffer, the counter being operative to send a signal to the controller to initiate processing of the stored samples by the data processor,"

as recited in Claim 1. Claims 2, 33, 43, 44, 57, 58 depend from Claim 1, and Claim 61 recites limitations similar to Claim 1. Thus, Claims 1, 2, 33, 43, 44, 57, 58 and 61 should be allowable over Kawabe.

The Office Action rejected Claims 4-6, 16-22, 27, 28, 50-52, 57 and 59 under 35 U.S.C. § 103(a) as being unpatentable over Kawabe et al. in view of Subramanian et al. (U.S. 6,459,883).

Subramanian also discloses "multiple fingers," each with "generic despreaders." See Abstract.

The Background and the Summary of the present application explains that multiple, dedicated processing elements, such the "multiple fingers" in Subramanian, assigned to process specific signal instances is inefficient, non-programmable, and not scalable to handle more signal instances, and increases complexity and costs. See e.g., Background p. 1, line 32 to p. 2, line 16.

Subramanian does not disclose or teach a single "data processor coupled to the first buffer and operative to (a) retrieve different segments of the digitized samples one segment at a time from the first buffer, each of the retrieved segments comprising one of the multiple signal instances, (b) process two or more of the retrieved segments one segment at a time with one programmed despreading sequence to provide despread samples, (c) decover the despread samples with a channelization code of programmable length to provide decovered symbols, (d) demodulate the decovered symbols to provide demodulated symbols, and (e) combine the demodulated symbols from multiple signal instances to provide processed symbols.

Subramanian also does not disclose or teach:

"a microcontroller coupled to the data processor and the controller, the microcontroller being operative to receive tasks from the controller, instantiate a state machine for each task, and direct the data processor to process the retrieved multiple segments; and

an address generator coupled to the first buffer and the controller, the address generator being operative to implement a counter to control a write address for writing digitized samples to the first buffer, the counter being operative to send a signal to the controller to initiate processing of the stored samples by the data processor,"

as recited in Claim 1. Claims 2, 33, 43, 44, 57, 58 depend from Claim 1, and Claim 61 recites limitations similar to Claim 1. Thus, Claims 1, 2, 33, 43, 44, 57, 58 and 61 should be allowable over Kawabe and Subramanian.

Drawings

Applicants submit that the above amendments to the drawings do not make any substantive changes or introduce any new material, but are simply the correction of typographical errors. Applicants further submit that the amendments are consistent with the specification as originally submitted. Therefore, approval and entry of the above amendments are respectfully requested.

Applicants have concurrently filed herewith a Letter to the Official Draftsperson submitting formal drawings to replace the originally filed formal drawings, including corrected drawing informalities indicated in this amendment.

Specification

Applicants have amended the specification by presenting marked up replacement paragraphs which identify changes made relative to the immediate prior version.

The changes made are primarily typographical or grammatical in nature, or involve minor clarifications of awkward wordings.

Applicants believe these changes add no new matter to the application and are fully supported by the original disclosure.

REQUEST FOR ALLOWANCE

In view of the amendments and remarks, Applicants submit that all pending claims in the application are patentable. Accordingly, reconsideration and allowance of this application are earnestly solicited. Should any issues remain unresolved, the Examiner is encouraged to telephone the undersigned at the number provided below.

Respectfully submitted,

Dated: January 7, 2005

By: ACC

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